Development of Electronic Test Infrastructure for the ATLAS LAr Calorimeter Off-Detector Readout System Upgrade

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1 Introduction

This summer, I had the privilege of participating in the joint program between the Canadian Insitute of Particle Physics and CERN that allows students to perform particle physics research in both Canada and Geneva. This involved two months working with the Canadian ATLAS Liquid Argon (LAr) team at McGill University in Montreal, Canada, and two months at CERN working with the ATLAS LAr Phase-II team, in part at the Electronics Maintenance Facility (EMF).

My contributions during this program were to the development of testing and troubleshooting tools for the upgraded electronics created for run 4 of the Large Hadron Collider (LHC), soon to be the High-Luminosity Large Hadron Collider (HL-LHC). This primarily consisted of performing tests on different Front End Link Exchange (FELIX) boards and creating troubleshooting documentation, as well as developing register monitoring scripts to troubleshoot the readout hardware.

2 Background

The Large Hadron Collider is the largest particle accelerator in the world that primarily aims to push the boundaries of fundamental physics and our understanding of the physical world. The LHC collides protons at extremely high energies, close to the speed of light, in order to collide them and probe smaller and smaller distances inside fundamental particles. These particles collide at four experiment locations along the 27 kilometre circumference of the LHC: CMS, ALICE, LHC-b, and ATLAS [3], which is the experiment I was working with.

ATLAS stands for A Toroidal LHC Apparatus is one of CERN's two general-purpose detectors.

This experiment is comprised of multiple sub-detectors and readout electronics that allow physicists to study the fundamental constituents of matter and their interactions [4].

One of these sub-detector systems, the Liquid Argon Calorimeter, is the main focus of the groups I was working with this summer. The calorimeters measure the energy deposits of the incoming particles resulting from the collision. These detectors have two components: lead to absorb the particle energy to slow them down, and liquid argon to measure that energy. The energy is measured via the collection of electron-positron pairs generated during this process [5]. The collection of signals from these electrons is already an immense amount of data to process as the events happen at a frequency of 40 MHz, or every 25 ns, and the amount of data recorded will only increase in the next few years as the LHC upgrades to the high-luminosity LHC (HL-LHC). The motivation behind this upgrade is to expand the physics program, increase the rate of collisions, observe more rare physics events, and therefore have more data recorded [2]. Given the age of the readout electronics at the LHC and the increased levels of radiation that will be seen during run 4 with a higher frequency of collisions, the Liquid Argon team is upgrading the entire electronics readout system.

Figure 1 illustrates the electronic readout system, where the blue elements represent on-detector electronics that need to be radiation tolerant, orange represents off-detector, and the Local Trigger Interface (LTI) clock signal block is purple to indicate that the signal gets propagated to all on- and off-detector parts in order to synchronize them together to a common ATLAS clock. Looking at the bottom half of the figure, the analog signal is first read on the calorimeter detector cells, then digitized, amplified, and shaped into a bipolar curve by the Front End Boards (FEBs). From there, the signal is sent to the Liquid Argon Signal Processor, where initial energy and time computations are made. The data is held in a buffer on this board while the Global Event Trigger Processor (GETP) determines whether to filter it out by searching for a Region of Interest while attempting to reconstruct the data and determine if they might be jets, photons, etc. This uses the aforementioned energy and time calculations. If the data is kept, it gets sent to storage where it can be further processed and filtered 'offline'. The Front End Link Exchange (FELIX) board acts as an interface between on- and off-detector functions, primarily forwarding the Local Trigger Interface (LTI) signal throughout the system. This helps to ensure that all the boards can talk to each other and have consistent timing information. The LATOURNETT board, which is the on-detector implementation of the Liquid Argon Timing System (LATS) board, manages the timing, configuration, and monitoring of on-detector boards. Finally, the Calibration board for ATLAS (CASA) manages real-time calibration of the FEB boards and the rest of the readout.

At the core of this upgraded off-detector hardware architecture are Field-Programmable Gate Arrays (FPGAs). They are ideal for prototyping custom data acquisition systems like this, as they can be easily reprogrammed to adapt to evolving needs. This flexibility, combined with the high-performance, ultra-low latency signal processing that FPGAs provide makes them well suited for this application [6]. Over the course of developing this system, there have of course been several iterations of each board as well as the setup shown in Figure 1. An older version of the FELIX board, the FLX-712, was developed for the phase-I upgrade and is used for troubleshooting and firmware development at different institutes. The newer version of the board, the FLX-182, is more similar to what will be used in run 4, but there are very few in circulation at the moment, while most institutes still have access to a 712. Other components of the readout system, like the LASP, must be tested alongside a FELIX board, and it's therefore important to benchmark the capabilities of the FLX-712 to be able to perform tests without multiple FLX-182s.

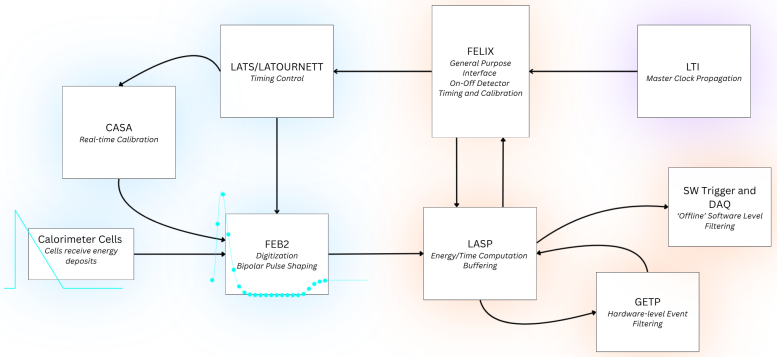

Figure 1: Flowchart of Electronics Readout System for the LAr Calorimeter

3 ATLAS at McGill: FELIX setup and LTI tests

3.1 Objective

At McGill, the electronics lab is in the process of creating a setup that can test the LASP boards that are being produced, for example to evaluate how they can send and receive signals from an important interface like a FELIX board. The objective of my work at McGill was to figure out how to configure and set up their FELIX-712 board to work with other boards in the lab, like AGILEX DevKits, and test the system functionality. Thus far, the FELIX board had not been successfully set up and the reason for that was unclear. Throughout this process, I created a detailed instructions and troubleshooting document for others that would use the FELIX later on.

3.2 Work Performed

The most interesting and rewarding part of this task was that the root problem was unknown, so my workflow had to consist of a lot of trial and error to learn about this particular piece of equipment. The FLX-712 hadn't been used much before in this lab, so the on-site knowledge was limited. The setup is represented in Figure 2, with a monitor that enables the user to connect to the Supermicro X11spa-tf motherboard which houses the FLX-712 board via pcie connection. Systematic debugging revealed that the upstream errors were caused by a register map (RM) mismatch between the hardware and the newer software version. Flashing an updated firmware image onto hardware with a mismatched RM can assign logic functions to incorrect FPGA regions, leading to non-functional hardware. While the board features a protection mechanism to block data transfers during an RM mismatch, this safeguard also inadvertently blocks incoming firmware updates. To resolve this chicken-and-egg issue, I investigated the underlying software command structure and built an environment that supplied the required execution parameters alongside legacy RM data. This allowed the firmware image to align properly with the hardware, re-establishing

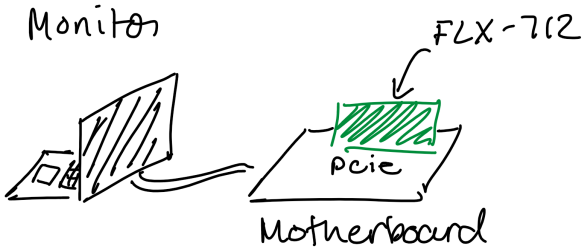

Figure 2: FLX-712 Setup at McGill University

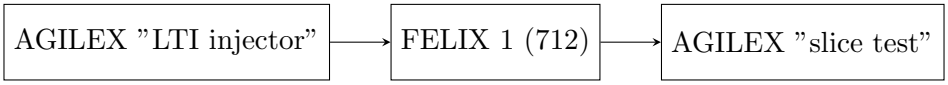

Figure 3: LTI Forwarding Test setup with DevKits

stable communication.

With communication restored, I performed tests to verify LTI signal forwarding through the FLX-712 board using two Altera Agilex 7 DevKits and firmware provided by Ricardo Luz (Argonne National Laboratory). These development kits provide a robust platform for high-performance FPGA designs similar to those used at CERN [1], allowing them to substitute for specific stages in Figure 1 since they use the same FPGAs as the LASPs that will be used in run 4. In the experimental setup (Figure 3), one Agilex board acted as an "injector" to generate the LTI signal, while the second board replaced the LASP to receive the forwarded signal. Signal integrity and functionality were verified using the Slice Test tool. These test results demonstrated that the FLX-712 board can reliably forward LTI signals and be used to test LASP functionality later on.

4 On-Site at CERN: FELIX Testing, Error Monitoring Scripts, ATLAS Dismantling

4.1 Objective

The Electronic Maintenance Facility (EMF) lab at CERN is a development space dedicated to testing and developing the LAr Phase-II components, such as the FEB, LASP, LATOURNETT, etc. My objectives while working on-site at CERN were to install the correct firmware/software on their FLX-712, verify its capabilities at the Elecronic Maintenance Facility (EMF) lab, develop error monitoring scripts for the LASP, and help with dismantling parts of ATLAS inside the cavern.

4.2 Work Performed

At EMF, I was able to replicate the same LTI forwarding test that was performed at McGill, with the same positive results. This test was an improvement from the previous one as we were able to use a real LTI signal and read it on a LASP board, as shown in Figure 4. This is an important

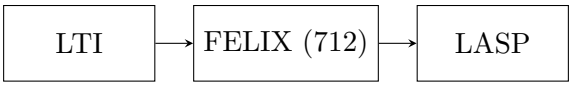

Figure 4: LTI Forwarding Test setup at EMF

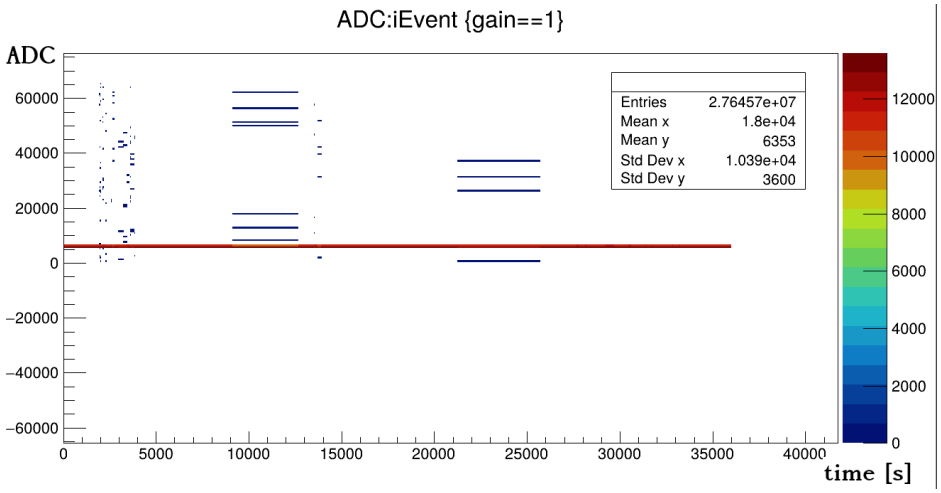

Figure 5: ADC Values shown out of range

result as previously, only the FLX-182 was known to be able to do this, and it is desirable to free up the only available FLX-182 at EMF at that time to use for data acquisition tests rather than LTI forwarding. This is because the 182 was developed for phase-II and will be more similar to what will be on the final version of ATLAS in the HL-LHC. Further tests were performed and confirmed that it is not possible for the 712 to forward the LTI signal while taking data from the FEB. This is an important capability limitation to have documented when planning tests with limited components.

The next portion of my work was to develop independent error monitoring scripts that probe registers directly for hardware troubleshooting. This is based on work that was already started by Victor Arredondo Quintana. The motivation for this was that some unexpected and not yet understood behaviour was noticed when taking data at the EMF. For example, the ADC values, which are the digitized values for an analog signal received from the FEB boards, can be seen outside their expected range $[5000, 7000]$ in Figure 5. This behaviour is seemingly random, lasting for seconds or hours, with a group of several channels getting 'stuck' at the same time but at different values. This issue was not isolated to any specific channels linking the FEB to the LASP. To locate where the issue was coming from, an optical splitter was installed on the FEB output and sent to two different LASP tiles. Much of the time the same issues were observed by both tiles, but there were many instances where only one of the two LASP tiles had an issue, which indicates that the problem is with that tile rather than the FEB. Another odd thing that can be observed in Figure 5 is that the values are constant, while it's expected to see fluctuations within a range as data arrives.

First, troubleshooting tools were added to the LASP firmware to monitor certain registers directly. In electronics, a register is a small storage unit that holds binary data. This can be anything from the state of a process (ready or not), memory addresses, or instructions. In this case, it was often error counters or status bits for various functions on the boards. Because registers are so low-level and the problem at hand was not understood, it offers a good starting point to get a big overview

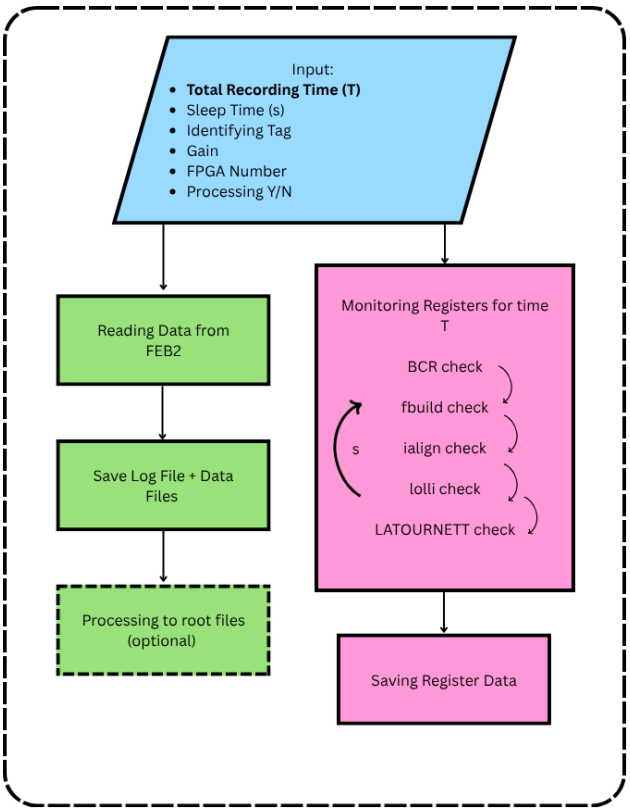

Figure 6: Register Monitoring Script Flowchart

of how the system is performing. From there, it was possible to write scripts that periodically read and save these values to be plotted with time. The hope was that some registers would start showing unexpected behaviour at the same time as the LASP, and this would isolate the problem. Figure 6 shows the structure of the monitoring code, which has been integrated into the data-taking partition at EMF.

The script is called with several inputs, only one of which is required: the total recording time. From there, register monitoring starts, which calls all relevant registers in a loop with sleep time s in between. In parallel, the LASP is recording data from the FEB as it normally would, none of the original functionality of taking data was changed.

An example of an early result from this error monitoring script is from a twelve-hour overnight test that was conducted while data was received from the FEB. Figure 7 shows the register values over time for the LASP bitslip, which counts up when the LTI connection is lost, and the LATOURNETT LTI validity. The absolute values of the bitslip register are arbitrary. The takeaway from this plot is that there are three points in time where two different parts of the readout system experience an issue: an invalid LTI signal. Investigating the LTI revealed there was a version issue that had compatibility issues with the rest of the system, and was promptly fixed.Going forward, having more errors correlated like these will help quickly isolate issues within the complex system so they can be resolved.

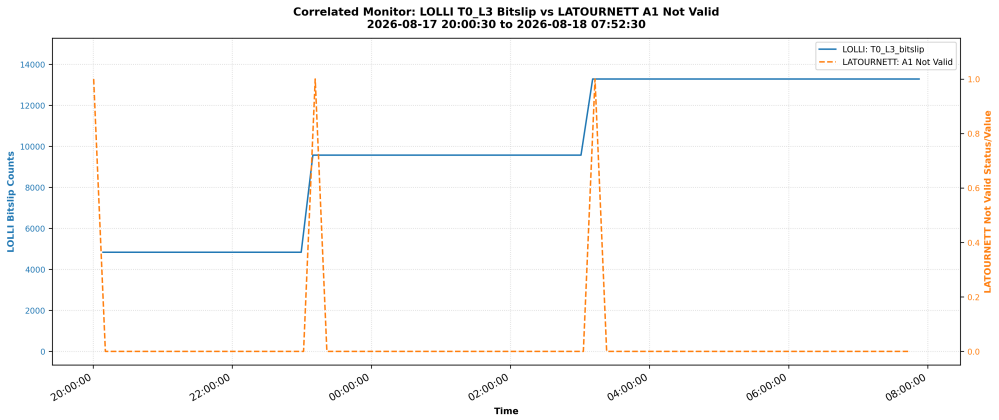

Figure 7: Correlated error monitoring from LATOURNETT and LASP

Finally, while it was much less technical work, I was able to go into the ATLAS server rooms underground with the dismantling team to help with the removal of cables, old electronics, and other equipment. Everything brought to surface was organized and set aside for recycling or reuse when possible.

Figure 8: Cabling Work Underground in ATLAS

5 Conclusion

Through the joint IPP-CERN program, significant contributions were made toward the development, testing, and troubleshooting of off-detector readout electronics for the ATLAS LAr Calorime-

ter Phase-II upgrade.

At McGill University, the initial roadblock regarding the FLX-712 setup was overcome by resolving register map version mismatches between hardware and software without compromising the FPGA. Subsequent validation tests using Agilex 7 DevKits successfully confirmed the FLX-712's ability to forward LTI timing signals. Upon transitioning to CERN's Electronic Maintenance Facility (EMF), this setup was validated with real LTI signals and a LASP board. Further testing established clear operational boundaries: while the FLX-712 is fully capable of LTI forwarding, it cannot simultaneously handle FEB data acquisition. Documenting this limitation provides valuable operational flexibility, allowing the newer FLX-182 cards to be reserved for full data acquisition tasks while enabling legacy FLX-712 boards to serve as test benches. Additionally, the development of direct register monitoring scripts integrated into the LASP data-taking flow now provides automated, real-time diagnostic capabilities to track down transient hardware glitches, such as anomalous ADC values. Participation in the underground cavern dismantling effort further provided a hands-on perspective on the physical scale and lifecycle of modern high-energy physics hardware.

This experience significantly expanded my understanding of field-programmable gate arrays (FPGAs), data acquisition (DAQ) architectures, low-level register communication, and systematic hardware troubleshooting within complex, large-scale physics experiments. Overcoming initial configuration barriers reinforced the importance of thoroughly understanding software-hardware interfaces during integration phases.

Looking forward, the functional FLX-712 setup established at McGill offers a solid local platform for ongoing firmware development and LASP testing. Meanwhile, the automated error monitoring framework deployed at CERN lays the groundwork for continuous run diagnostic routines, aiding the team in pinpointing and resolving remaining hardware instability on the LASP boards prior to the High-Luminosity LHC Run 4 deployment.

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