ITk Strips Module Testing, and FELIX Test Stand Building for ATLAS Detector for HL-LHC Upgrade

Kaitlyn Liang
Supervisors: Karola Dette, Olivier Arnaez, and Richard Teuscher

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1 Introduction

The ATLAS detector is a general detector used to study proton-proton collisions created from the Large Hadron Collider (LHC). The detector consists of the Inner Detector, the Calorimeters, the Muon Spectrometer, and the magnet systems. The purpose of the Inner Detector is to track the charged particles' trajectory with the use of silicon detectors. The calorimeters measure the energy of photons, electrons, and quarks. The muon spectrometer measures the tracks of muons. The magnet system create a magnetic field that causes charged particles to bend, and allows the momentum to be measured.

In 2026, the LHC will be upgraded to the High-Luminosity LHC (HL-LHC). The beam will be 14 TeV, and the nominal collision rate will increase by a factor of 5. As a result, a larger data sample will be taken; leading to results with lower uncertainties. Due to the increased luminosity, a large number of tracks will be produced. Therefore, the silicon detectors of the Inner Detector need to exhibit a higher granularity to accurately distinguish and reconstruct the tracks. Additionally, the increased amount of data collected requires increased trigger rates and a larger readout bandwidth. Lastly, the silicon detectors need to have an increased resistance to radiation damage due to the radiation caused from collisions.

As a result, the semiconductor tracker system (SCT) and the Transition Radiation Tacker (TRT) will be replaced by the Inner Tracker Detector (ITk). The ITk will consist of pixel and strip silicon strip detectors. Currently, the silicon strip modules are in the prototype building and testing phase. More tests need to be completed in order to ensure the quality of the detectors.

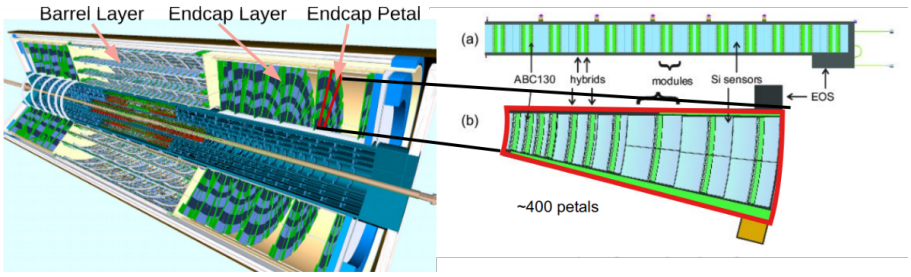


Figure 1: Layout of the Inner Tracker (ITk)

Since new silicon detectors are needed, a new way to process data, and signals have to be established. In the current Trigger/DAQ system, the data from the front-end electronics go through a readout driver. The purpose of the readout driver is to capture the time and position of a track, and format the data. The data then travels through a readout system, and it is then redistributed to a high-level trigger farm. To maximize the processing power and bandwidth of the system, the Front-End LInk eXchange (FELIX) board is used to create an interconnect the front-end electronics and the commodity network. At the time, the FELIX Test Stand Set-up is being installed and configured at CERN. More adjustments and debugging need to be done in order to perform procedures to test and calibrate the silicon detector modules

As part of the IPP Student Fellowship Program, I spent May and June in Toronto working with the University of Toronto ATLAS group there on Module Testing for the ITk Strips. I then spent July and August at CERN working on the ITk FELIX Strip Test Stand. As a result, my report is split into two components: Silicon Module Testing in Toronto, and building the test stand at CERN.

2 Noise Level Comparison for Silicon Detector Modules for ATLAS Inner Tracker Upgrade

2.1 Design of the ITk Strip Detectors

The Inner Tracker is composed of silicon detector modules. The ITk strip detectors are composed of 4 barrel layers, and 6 end-cap layers on each side. The end-cap has a disk shape, and are built by joining multiple petals in a circle. Each petal is an assembly of 6 different modules. Each module consists of a silicon sensor, 2 or 4 hybrids (depending on the module), and a powerboard.

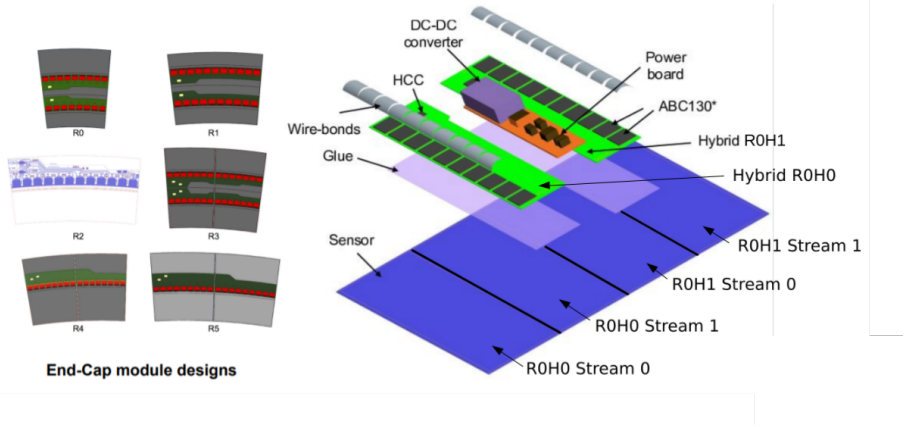


Figure 2: Modules composing the endcap, and layout of the R0 Module

The silicon sensors in the ITk will undergo a large amount of radiation, and this will greatly affect their properties. An n-type silicon semiconductor is an extrinsic semiconductor doped with electron donor atoms while a p-type silicon semiconductor is doped with an electron acceptor atom. Damage to the bulk silicon will increase the depletion voltage to over 1000 V. Damage on the surface will cause the charge on the oxide-silicon interface to increase. Due to type inversion, p-type bulk is used, and the readout chips must be n-type implants. Therefore, the sensors are n+-in-p sensors.

The n+-type implants are arranged in long strips arranged in a fan geometry. There are 4 or 2 rows of strip segments. Each strip represents a channel, and there are 128 channels read out for each readout chip. There are about 7-12 ABC130 (ATLAS Binary Chip for 130 nm) Readout Chips on each hybrid as well as an HCC (hybrid control chip). While HV is used to reverse bias the silicon sensor, LV is used to power the readout chips. The power board powers the AMAC (Autonomous Monitor and Control) chip, and includes a higher voltage to 1.5 V DC-DC converter for the ABC130s.

2.2 Quality Control Tests on ITk Strip Detectors

When a charged particle passes through a channel on the silicon detector, the signal is recorded in the ABC130s, and the data is transported through the HCC and an FPGA board to the Inner Tracker Strips Data Acquisition software(ITSDAQ). For a channel, a threshold must be established for a certain charge in the sensor. Theoretically, a varying threshold value vs efficiency plot would look like a step function at the threshold value. However, due to noise, the plot looks more sigmoidal. The vt50 is the value where 50 percent of all hits are registered, and the noise width quantifies the slope of the threshold scan. To confirm proper read-out from the ABC130s, the threshold value of a signal is varied at a given injected charge, and the efficiency of registered hits is measured.

When the threshold scan is done for many injected charges, the gain of the channel can be determined. Using the gain and the noise width, the equivalent noise charge (ENC) is calculated. The ENC is a quantitative value to the larger noise one gets from an increase in charge. ENC is often used as the 'noise' level because the charge does not have to be standardized.

$$ENC = \frac{noisewidth}{gain}$$

When 3 different charges are used to determine the equivalent noise charge, a "3 Point Gain test" has been completed. A "10 Point

Gain test" occurs when the same test is completed with 10 different charges. The 10 Point Gain test can be divided into a low statistics and high statistics test, and these tests are distinguished by the number of triggers applied. Other tests include: a Strobe Delay (calibrating the time delay when the command is sent and when it is actually sent), a Trim Range (adjusting parameters of each channel to reduce the noise and variation in the channels), and Noise Occupancy (threshold scan with no injected charge).

2.3 Goal and Method

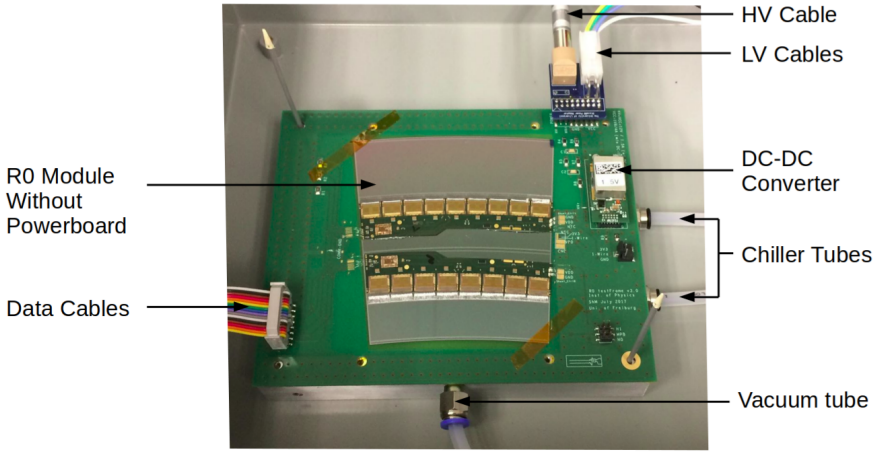


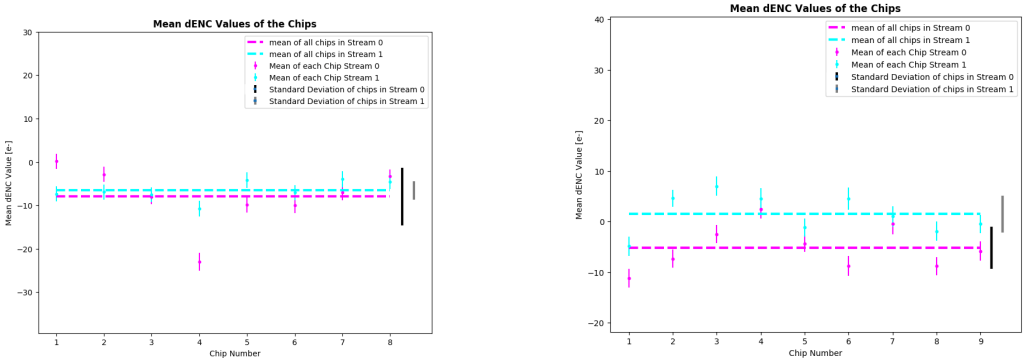
Figure 3: Set-up of the R0 hybrid in the University of Toronto cleanroom

The ENC of individual channels on the ABC130 chips can change depending on the environment of the module such as temperature or new electronic components. Therefore, a way to quantitatively determine the existence of a significant change in noise levels between two different environments is needed. A program in Python was constructed to first graph the ENC levels for each stream of each hybrid for both trials. The next graph plots the difference in ENC between the two trials. The noise values are put into a histogram for each individual chips. A Gaussian distribution can be plot, and the mean and sigma values for each chip is calculated as well. These values are then put on another plot to compare the

difference in noise for each chip and stream. The 3 Point Gain, 10 Point Gain(low statistics) or 10 Point Gain (high statistics) is compared between the two modules, and these tests are completed after the Strobe Delay and Trim Range tests. The full output of the program is shown in Appendix A. All measurements were done on the lab set-up in Toronto, Canada. The modules used to conduct the tests were TO1R0, and TO2R0; the first, and second, and third R0 modules built in Toronto.

2.4 Results

In order to get acquainted with the software, a "DAQ load" was first used to practice running the tests. A "DAQ load" is a module without the silicon sensor. The first test was conducted on TO2R0, and the HV was varied between -100V and -300V. 3 Point Gain tests were completed at each voltage, and compared. The mean difference in ENC values for each chip and hybrid are shown in Fig. In this sample, the overall dENC value for all chips tend to be rather low (from 0-20 electrons). There appears to be a wider range of dENC values for Stream 0 for both hybrids. However these differences are insignificant because the standard deviation is relatively large. Therefore, there is no significant change in ENC values when the HV varies from -100V to -300V. The result is expected because the sensor should be fully depleted at -100V, and the noise levels would change if that is not the case.

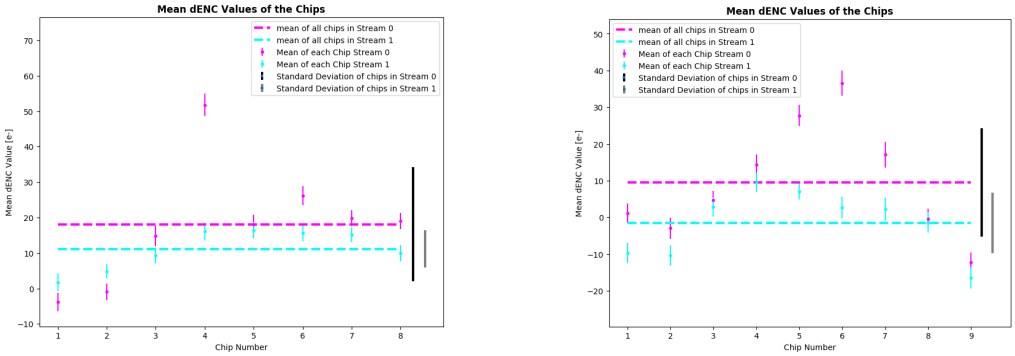


(a) R0H0 Hybrid (b) R0H1 Hybrid

Figure 4: Mean dENC Values for Chips in TO2R0 Module after the addition of a chiller

The second test was also conducted on TO2R0, and the addition of a chiller at 10 C was added. Although the chiller is set to 10 C, the module is about 15 C due to the space between itself and the chiller. The temperature probe is currently positioned even farther from the module and the source, so its readings are not accurate. The mean difference in ENC values for each chip are shown in Fig.

Most of the chips exhibited similar means and sigmas; indicating no significant change in the addition of a chiller. Although temperature does affect the noise levels of silicon sensors, the difference in temperature is most likely too small to significantly change the noise levels.

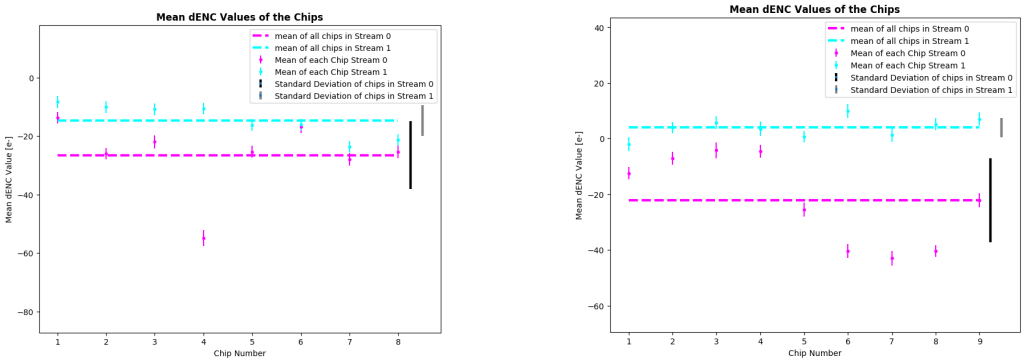


(a) R0H0 Hybrid (b) R0H1 Hybrid

Figure 5: Mean dENC Values for Chips in TO2R0 Module after the addition of 200 V

The third test was the addition of the powerboard in comparison with 2 different modules. A 10 Point Gain test was conducted for TO1R0 (without the powerboard), and TO2R0 (with powerboard). For TO1R0, two of the chips in R0H1 have malfunctioned, so the R0H0 hybrid is compared. The program does filters out differences in ENC more than 3 standard deviations away from the mean because sometimes channels do not exhibit any signal due to the trimming. However, it appeared the TO1R0 module exhibited lots of variations in noise levels, so not all the dENC values due to the lack of signal in a channel were cut. As a result, the dENC levels exhibited very large values in certain chips, and the Gaussian fits exhibited significantly higher chi square values. This test verifies a limitation on the program made; data with lots of variation in noise levels will not be accurately evaluated. Additionally, this test shows that this program is best suited for comparing the same module as opposed to different modules. The results are shown in Appendix B.

The last test was the addition of the powerboard comparing the same module. In October of 2018, the powerboard was installed on TO2R0, so data from a 3 Point Gain test was taken before and after the installation of the powerboard. Most of the streams exhibited a similar mean and sigma, and the dENC values are greater in magnitude than the dENC values calculated after the addition of the chiller and the change in HV. The larger dENC values are expected because an electronic change is more likely to influence noise levels than environmental changes.



(a) R0H0 Hybrid (b) R0H1 Hybrid

Figure 6: Mean dENC Values for Chips in TO2R0 Module after the addition of a powerboard

In conclusion, there is no concrete evidence that the change of temperature of about 10 C and the addition of a power board causes a significant change in ENC levels. These tests were mainly done on one module, and these tests need to be done on more modules to get a more conclusive answer. Additionally, the comparison program is useful in showing how noise levels for each chip varies under electronic or environmental changes. If noise levels are quite variable (such as chip 4 stream 0), that chip can be replaced.

3 ITk Felix Strip Test Stand Building

3.1 Purpose

In the current Trigger and Data Acquisition System (TDAQ) in the detector, the front-end electronics are each connected to a read-out driver, and these cards are used to implement data processing functionality. They are then separately connected to individual Readout Systems that convert the events into signals. Lastly, the Readout Systems are connected via Ethernet to the High-Level Trigger Processing Units (HLTPU), and these units perform the duties of the trigger.

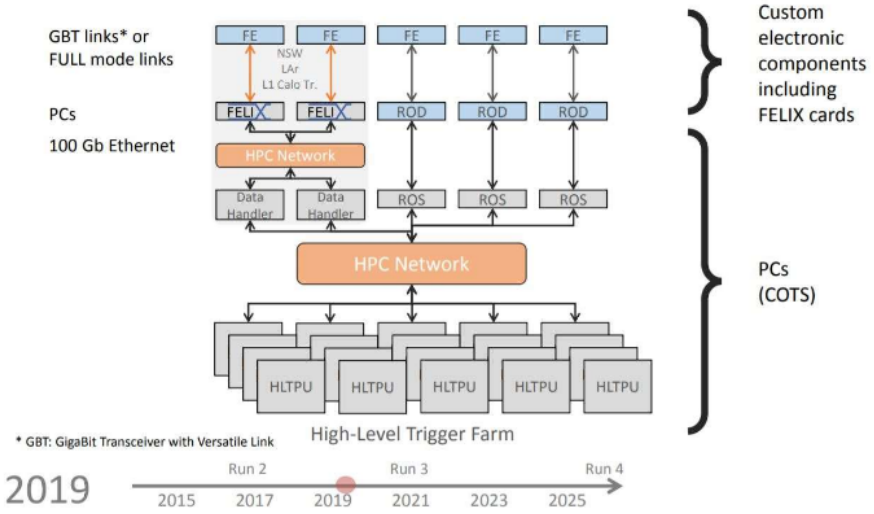


Figure 7: Trigger and Data Acquisition Systems for the ATLAS Detector in 2019. It is important to note that all the components of the ATLAS Detector will incorporate the FELIX system. As shown, FELIX is already being incorporated in some systems such as the L1 Calorimeter. The Felix upgrade for the ITk strips will occur in 2024.

However, it is important to note that these systems are built for a certain nominal rate, and if the rate is exceeded, the TDAQ works less efficiently. By working less efficiently, bottlenecks are sure to arise. For example, a larger number of collisions resulting

in tracks in the forward direction will have a slower processing rate while the readout systems corresponding to the central tracks will not be used. As a result, a network is needed to connect and allocate data from the front-end electronics to the readout drivers. Hence, the Front End LInk eXchange (FELIX) system serves as the interface between data acquisition, detector control, and Timing, Trigger, and Control (TTC) systems, and it is used to maximize the bandwidth of the processing. FELIX will serve as a router between front-end electronics and data collection and trigger systems. The FELIX system will be implemented for all components of the ATLAS detector at varying times, and the ITk FELIX Readout System will be installed in 2024.

3.2 Set-Up

Currently, the goal is to create a working FELIX set-up at CERN for the ITk Strips. The FELIX Test Stand should be able to conduct the same tests as ITSDAQ used before. The FELIX Test Stand consists of the hybrids, the Scalable Low Voltage Signalling (SLVS) board, the Gigabit Transceiver (GBTx) board, and the FELIX card. The hybrids consist of an HCC, and a large number of ABC130 chips. There are many registers to control the parameters of the HCCs and ABC130s. Both the HCC addresses, and the Chip IDs can receive and send data to the readout system, and the each chip is distinguished by the HCC address and Chip ID. The hybrids are connected to the SLVS board via the ethernet cables. The SLVS board is responsible for shaping and amplifying the signal from the readout chips. The SLVS board is not necessary if the signal from the chips is strong enough, and this is dependent on the length and quality of the cables.

The SLVS board is connected to the GBTx board by ribbon wires. The GBTx board is a radiation tolerant chip used to provide bidirectional optical links to the FELIX board. Optical links are used to limit the noise levels over long cable lengths. A single optical link is able to merge and simultaneously be used for the three logical paths of the TTC, DAQ, and Slow Conrol (SC) information into "electronic links" ("e-links"). It is important to note that the

hybrids, and the GBTx boards are in the detector while everything else is out of it.

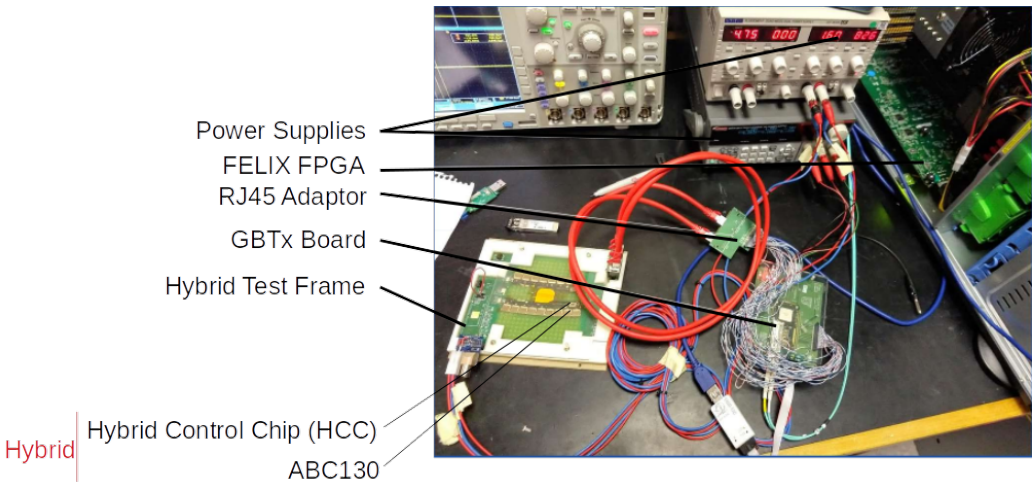


Figure 8: ITk FELIX Strips Test Stand with the R0 encap module

The optic cables connect the GBTx board to the FELIX FPGA. An FPGA stands for Field-Programmable Gate Array, and it is a CPU that is reprogrammable after manufacturing. The FPGA frameware allows FELIX to sort and store data in the right buffer. YARR is the program used to program FELIX, and when programmed to, FELIX is able to take out a specific set of data, and exchange it with the computer it is sitting into.

3.3 Work and Progress done on ITk FELIX Strip Test Stand

At the start of July, the set-up included an R0 endcap module with 2 hybrids with HCC addresses 5 and 6. There is no data being sent from HCC 5, and no commands could be sent. At the hybrid's connection to the ethernet cables, probes can be put on pins to display the electrical signals that make up the startup pattern. It is important to note that a green adaptor board is attached to the blue SLVS board to establish the establish the electrical link with

the hybrids through ethernet cables. When probes are put on pin 9 and 10 (the corresponding pins to HCC 5) of the green board, the 0s are low and the 1s are high. This should be the opposite way around; thereby indicating an inversion in the SLVS board. Since the interleave was written for non-inverted cables, the data could not be interpreted. As a solution, new adapters were received so the inversion did not occur.

Even though the inversion was fixed, only some data from YARR was observed, and these results were very unstable. It was noticed that a large voltage drop occurred from the power supply to hybrid, so a DC-DC converter would be ideal for this set-up. To reduce this drop, the power cables were shortened, and a gray ribbon cable was substituted for the ethernet cables. With these adjustments, the data from HCC 5 produced consistent and expected results. It is important to note that data comes from e-links 0 and 1 if the source is HCC 5, and e-links 5 and 6 if the source is HCC 6.

Although HCC 5 started working, data could not be received from HCC 6. Since data would come from HCC 6 occasionally upon randomly changin the combination of phases for the 320 and 160 MHz clocks, a loop was written to try every possible combination of phases. However, the working combination would change each time the program was run.

Since there were no other possible solutions to explore, a new version of the firmware (rm4.4), and an updated version of Vivado (Vivado 2018.3) was installed. A new source code for the new firmware version was downloaded, and an installation with more options was downloaded. After many tries, Vivado was able to be recompiled. After changing the position of the trigger and the phases, repeatable and reliable data was seen for both HCC 5 and HCC 6.

Once data could be read from the HCC addresses, data from the ABC130 chips need to be read. Chips 22 and 26 were able to read, but none of the other chips could. Due to the daisy chain

connections, chips 23 and 25 are suspected to be burnt out from previous measurements and the absence of a DC-DC converter. Chips 16 and 19 could not be read out either. A Strobe Delay Scan was conducted, and completed after a longer than expected time. The delay in completion may be due to the malfunctioning of several chips. All the other tests such as 3 Point Gain tests and Noise Occupancy scans could not be completed. Under most circumstances, we would look into the malfunctioning of the tests, but our module was already barely functioning. Additionally, the modules with the new ABC130 Star chips were arriving shortly, so it was decided to move on to configuring a versatile panel of hybrids.

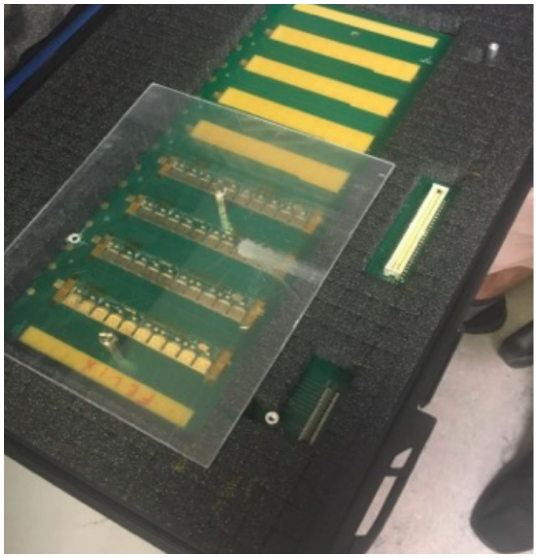


Figure 9: ITk Strips Barrel Hybrid Readout Panel

The panel consists of three working barrel hybrids that can be measured simultaneously. As a result, another power supply is needed, and that was added to our set-up. At first, multiple types of cables were used to power the hybrids due to convenience. However, a thinner type of cable tended to exhibit a larger voltage dorp, so that was swapped out. The SLVS board was taken out because the signal was large enough as is. The HCC addresses were able to

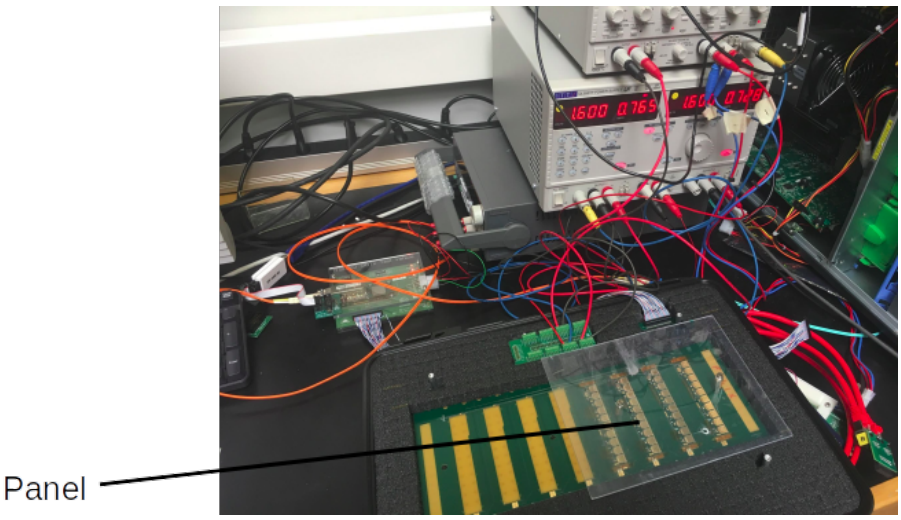


Figure 10: ITk FELIX Strips Test Stand with the panel of barrel hybrids

be read out from the probes as HCC 17, 18, and 19. At first, the ABC130 chips could not be read, and it was suspected to be due to the differences in daisy chain wiring between barrel and endcap hybrid configurations. After the configurations were change, they still could not be read. However, an increase in current is exhibited whenever a chip is configured, and from the increases in current, the chips were able to be configured.

3.4 Next Steps

Firstly, the ABC130 chips on the panel could not be read out, so that would be the immediate next step. Secondly, a new FELIX Test Stand will be built once the ABC130 Star modules are delivered to CERN. The modules are expected to arrive in early September. Once the new set-up is in place, the same goal to conduct the same tests from ITSDAQ will continue.

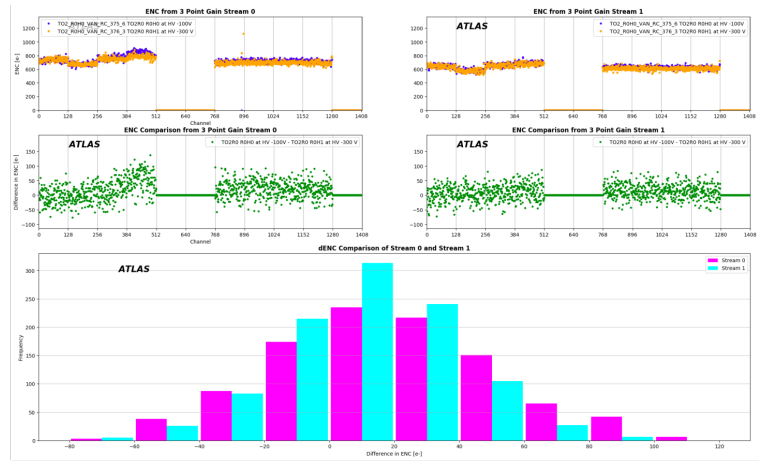
4 Acknowledgements

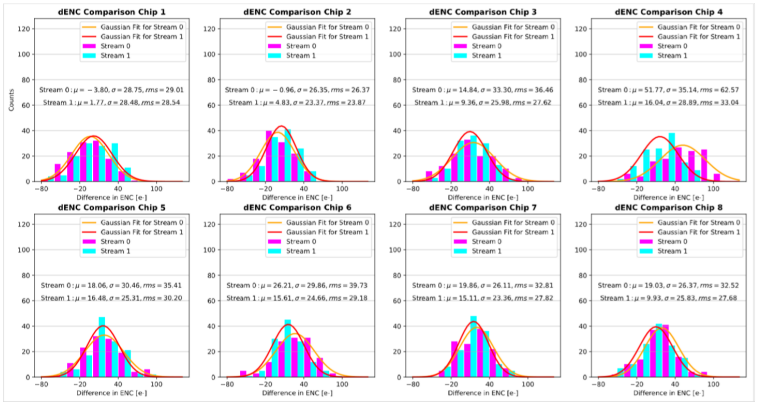
Over the past 4 months, I have received help and guidance from so many amaing people. Firstly, I would like to thank my supervisor, Professor Richard Teuscher, for his guidance and giving me this wonderful opportunity. In Toronto, I mainly worked with Karola Dette, and her expertise, and help were so beneficial to my project. Additionally, Professor William Trischuk gave lots of guidance and support throughout my time there. At CERN, I mainly worked with Olivier Arnaez, and his help was key to any progress in my project. Additionally, the other members of the ITk FELIX Strips Test Stand (James Beacham and Elise le Boulicaut) were extremely helpful and informative.

Secondly, thank you to Steven Robertson, Peggy White, and all the members of the Institute of Particle Physics who keep the program running. Additionally, thank you to the CERN Summer Student team of Eszter Badinova, Ana Dordevic, and Adriana Bejaoui. It has been the most incredible experience, and I am so grateful to take part.

5 Appendices

5.1 Appendix A





Chip #	Stream 0 mu		sigma	rms	Number of Channels	Stream 1 mu		sigma	rms	Number of Channels
1	-3.80	28.75	29.01	128		1.77	28.48	28.54	128	
2	-0.96	26.35	26.37	128		4.83	23.37	23.87	128	
3	14.84	33.30	36.46	128		9.36	25.98	27.62	128	
4	51.77	35.14	62.57	128		16.04	28.89	33.04	128	
5	18.06	30.46	35.41	126		16.48	25.31	30.20	128	
6	26.21	29.86	39.73	128		15.61	24.66	29.18	128	
7	19.86	26.11	32.81	128		15.11	23.36	27.82	128	
8	19.03	26.37	32.52	128		9.93	25.83	27.68	128	

Figure 11: Other Graphs, and Data Generated by the Noise Comparison Program for the HV at 100 V vs 300 V Comparison

This image displays the other plots, and data generated from the program made to compare noise levels of ITk strip modules.

5.2 Appendix B

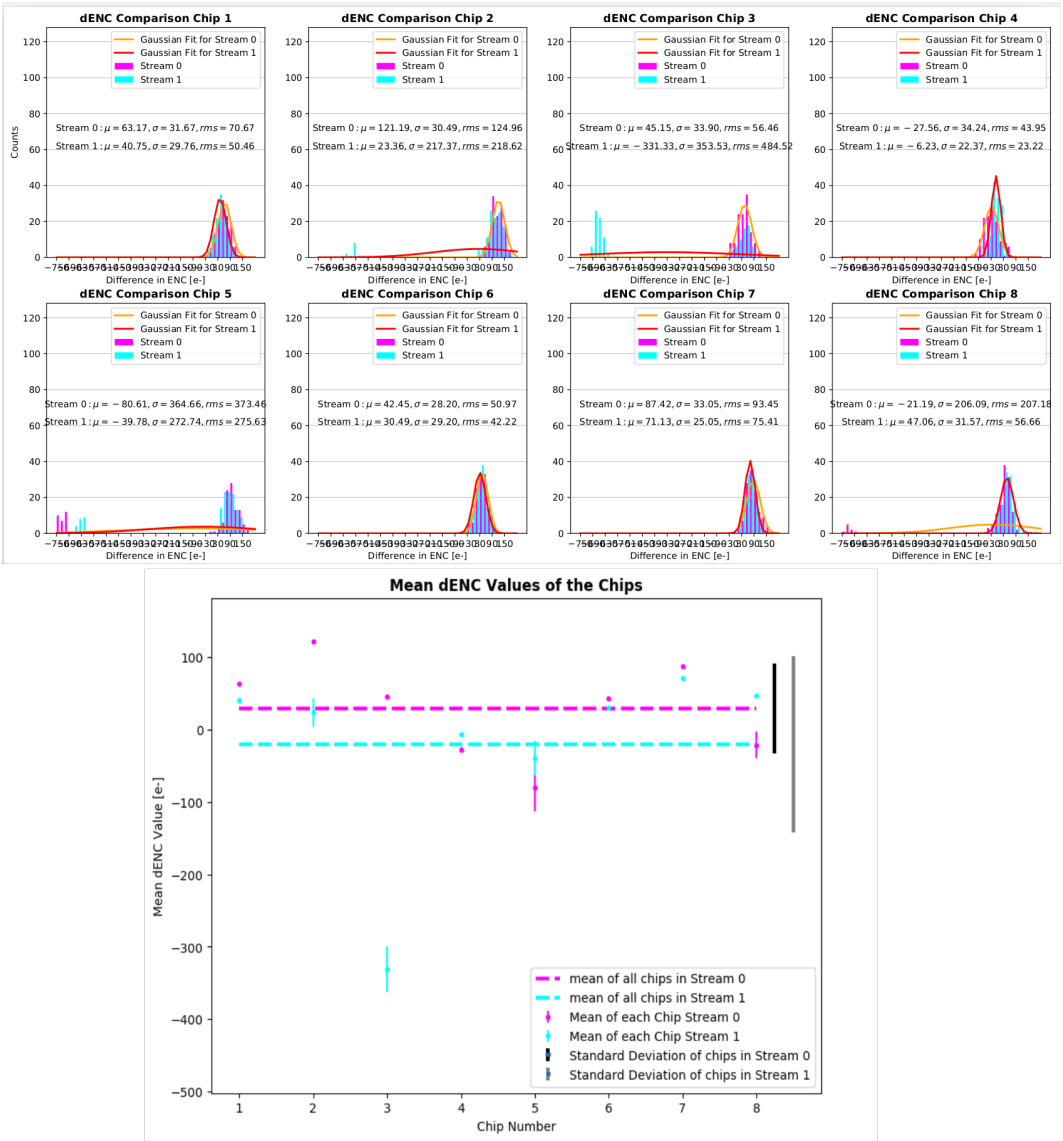


Figure 12: R0H0 output for the TO1R0 vs TO2R0 with the addition of the powerboard.

These are the Gaussian fittings for each chip readings in the R0H0 Hybrid. As shown, the Gaussian fittings do not fit the data prop-

erly due to a group of outliers. As a result, the means and the sigmas will be inaccurate.

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[2] Carlos Garcia Argos. *ATLAS ITk Strips DAQ System With 130 Chipset: User and Troubleshooting Guide*. CERN. 23 November 2017.

[3] David Griffiths. *Introduction to Elementary Particles*. Wilen-VCH GmbH Co. KGaA, Federal Republic of Germany, 1998.