

ITk Pixel Sensor Module Assembly

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Abstract

The short report below details my work as a CERN summer student from July to August 2024. My job involved the assembly of modules for the Inner Tracker for the ATLAS experiment, which is needed for the High Luminosity upgrade to the LHC. I focused on the quality control(QC) and assurance(QA) of incoming modules and pieces as well as streamlining the testing procedures. This involved both lab work to test incoming parts and development of Graphical User Interfaces (GUI) for already existing processes.

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1 High Luminosity LHC Upgrade

1.1 ITk Upgrade

The ATLAS detector is one of two general-purpose detectors at the LHC. It is designed to study high-energy collisions produced within the accelerator.

The LHC is planned to be upgraded to the High-Luminosity(HL) LHC. This upgrade will result in an increased number of collisions and consequently in radiation. These new conditions will help with future research and discoveries, however, they pose challenges to current detector technology in ATLAS. As a result, the ATLAS detector will undergo several updates. The focus of this short report is on the Inner Tracker(ITk), which will serve as a replacement for the current Inner Detector (ID) which has been in since the beginning of operations.

The detector is divided into 2 main geometries, barrels (horizontal) and end-caps (vertical). Barrels are cylindrical shells of sensors aligned along the beam axis, making them optimal for detecting low-rapidity events. Meanwhile, end-caps are a circular combination of sensors placed perpendicular to the beam axis, making them better for events with large rapidity.



Figure 1: Cross Section of ITk [3]

Like the Inner Detector(ID), the ITk uses silicon sensors. For increased granularity, pixel sensors (red, Figure 1) are placed in the inner layers of the ITk, while the outer layers use longer strip sensors (blue, Figure 1).

1.2 Module Assembly and Testing

The pixel modules must meet strict criteria to be placed into the ITk. They are tested at every step of the assembly process to find assembly steps that decrease module yield.



Figure 2: Assembly flow of pixel sensors from bare module to final module. Gray steps are completed, Outer Barrel(OB), Orange represents an assembly step performed by outside contractors [7]

Tests of the physical and electrical properties of modules are performed after any modification is made. The full development cycle can be seen in Figure 2.

1.3 Pixel Sensors

The basic pixel unit is a $50x50 \ \mu m^2$ (pixels closer to the beam line have $25x100\mu m^2$) silicon sensor. An array of silicon sensors is then bump-bonded to a front-end chip(FE) to create a hybrid bare module. The FEs integrate and digitize the charge from particle tracks in order to give a readout. Single, dual, triplet, and quad hybrid modules exist and are differentiated by the number of FE chips they use. The number is as the name would imply. All are connected to a single sensor array, the array is sized according to the type of module. For example, a sensor for a single module will be about 4 times smaller than for a quad module.

The bare module is then completed into a full hybrid module by adding a PCB(printed circuit board). The PCB is glued to the top of the front-end chip and electrically connected to it by a wire bonding. The PCB provides power to reverse bias the sensor and relays data from the FE.

As a group, the module works as follows. The PCB allows reverse biasing of the pixel sensors, a particle crosses the sensors releasing charges. The charges are collected on either side of the sensor and a signal is created and digitized by the FE chips which is then relayed by the PCB.



Figure 3: Full Pixel Module(flex)

2 Reception

The most important parts of the ITk, hybrid bare modules, are received from outside vendors. As such, they must be inspected to ensure their quality and to notify the manufacturer of any issues identified.

2.1 Hybrid Module Visual Inspection

Visual inspection occurs as soon as hybrid modules are received from vendors and so fall in the bare module reception section of the assembly flow displayed in Figure 2.

Using a 3D imaging microscope, the front and back surfaces of the sensors are examined for any damage or contamination that would affect their functionality. Certain issues are minor, such as debris on the sensor or minimal abnormalities (left Figure 4). However, larger issues such as major scratches, tears, or contamination can also be found (middle and right Figure 4). Any potential damage is imaged and cataloged for future reference. These images are sent back to the manufacturers so that flaws in the production can be addressed and fixed.

Figure 4 is a special inspection of only FE chips. They were known to be damaged during manufacturing before being joined with the sensors.

When modules (or FE chips in special cases) are found to be damaged, they cannot be put in the ITk. However, they are not discarded either. They can then be used to test and develop different recovery methods, such as plasma cleaning. These will usually not save heavily damaged sensors, but those can still be used to test the methods.



Figure 4: Reject FE Chip Visual Inspection

2.2 PCB Metrology

Since the ITk must fit thousands of modules, there are stringent regulations on the sizes of each part to ensure good coverage and proper fit. PCB metrology specifically, occurs in the Module PCB reception section from Figure 2

As the flexes are received from manufacturers they must be measured and compared to their fabrication drawing to ensure that they meet specifications. For PCBs, the technical drawing can be seen in Figure 6.

The measurements were performed using a 3D profilometer. The PCBs are carefully transferred onto a jig and then pulled down flat by a vacuum. The profilometer is calibrated to the height of the jig, so it measures thickness as the elevation from the reference plane. It uses this data to return a topological image of the PCB shown in Figure 5(Left).



Figure 5: Profilometer Scan Results(Left) and Dimensional Measurements(Right), PCBs are upside down in scan

The width, height, and thickness of the PCB are obtained from this scan. The thickness measurement is taken by finding the average of the contact pads(red circles Figure 5 left) as these should be the most elevated parts of the PCB. The width and height are mea-



Figure 6: PCB Fabrication Drawing [1]

sured by going across the PCB. The start point is chosen as the point where the elevation measurement increases relative to the reference plane(i.e. when the PCB's thickness is first measured), similarly, the elevation readings returning to zero(reference plane) signify the end of the PCB.

The connections to the PCB frame must be avoided when making these measurements as they have thickness and will mask the starting point of the actual PCB. The areas covered by the connections are removed from the scans in Figure 5. Furthermore, the start(end) of the PCB is expected to be marked by a clean sharp increase(decrease) in elevation. If any edges are found in this region another point must be selected.

The measurements are then compared to the specifications of the fabrication drawing. Figure 6 shows that the height and width of the PCB must not exceed 40.60 ± 0.1 mm and 39.60 ± 0.1 mm [1] respectively. Any sensor that falls outside of these ranges is marked as unsuitable.

3 GUI Development

ITk is currently in the pre-production phase. As such, tests, programs, and methods are still being developed and fine-tuned. Most of these still require command-line inputs to run and collect data. This process is tedious, time-consuming, and error-prone. The development of GUIs streamlines this by decreasing the amount of user inputs and required system knowledge.

3.1 Backside Metrology

A new module flatness testing setup, called Backside Metrology, was recently developed. This station measures a bare module's thickness. This will be used in the Bare Module Reception part of the production flow in Figure 2.



Figure 7: Backside Metrology Setup

This test does not require many user inputs to run properly. By far the most important input is determining the size of the scan and how many points should be collected. This functionality is in the "Edit Parameter" button(Figure 8). This allows the user to customize the scan to their specific module.

This window was designed to be as simplistic as possible. The user should easily know which input corresponds to which value. When the window is opened, the current parameters are displayed, this allows the user to check their setting easily before running the tests. A default parameter button is included because most modules should be tested identically. The exact parameters have yet to be determined, but can easily be modified in a csv file. The GUI also forbids any input that would crash the code. This includes negative values, positions that are out of range, resolutions of zero, and non-number inputs. As can be seen in Figure 8.



Figure 8: Backside Metrology GUI

For bookkeeping purposes, it is required to input the module's Atlas Serial Num-

ber(ASN). The test will not run otherwise and a prompt will be displayed. The "Show Analysis" button displays a 3-dimensional plot that shows the height elevation of the module in comparison to the reference plane(Figure 9). This plot can be used to visualize where issues might be located and is especially useful right after a scan.

If an ASN already exists, it cannot be used again. A similar prompt to the missing ASN will be displayed. This assures that there is no confusion later on. It is also useful because the "Show Analysis" button uses the ASN input to determine which plot to show. This allows the user to review old scans as well as current scans and can be used to assess the improvement of sensors over time. If the name is not precise enough it will warn the user that more than one file with a similar name exists.



Figure 9: Elevation Plot, the grid is the reference plane split into $1 \times 1 \ \mu m^2$ squares, the blue dots represent the elevation readings

Finally, when the process is completed the data is analyzed to determine if the module is within specifications. Modules are then assigned a pass or fail value based on this information. Along with other information such as the test time, the GUI arranges this data in a predetermined CSV format for ease of access.

3.2 Electrical QC Tests

Electrical tests are run on modules to assess sensor performances. This occurs after the flexes are attached to the bare modules and wire-bonds are added, in the Initial QC test section of Figure 2 These tests are more complex than the backside metrology and have more parts and dependencies to take into consideration. A GUI is convenient here because it puts all the possible actions in one location. The user can visualize which tests are active and proceed as necessary. This minimizes the chances of human errors which is critical since errors here will severely damage sensors.



Figure 10: Main Window of Electrical Test GUI

3.2.1 Chiller

As the name implies, the chiller controls the operating temperature during electrical testing. The electrical tests can be run in warm(20°C) and cold (-40°C) temperatures. This is because, the ITk will be cooled while in operation, yet due to the extreme environment temperatures may still rise. Sensors must be able to operate in both conditions, however, it should be noted that the cold is the optimal temperature for operation.



Figure 11: Chiller GUI

Other than starting and stopping the chiller, the user may also want to regulate the temperature of the setup. The user can set the new target temperature within the bounds defined above. Since the chiller takes time to warm up and cool down the testing environment, the internal temperature of the readings can be fed to the GUI to show the current temperature. There is also, the time of display to make the user aware of the accuracy of the information displayed.

One of the main considerations of this part of the GUI was selecting how to display the temperature of the sensors. One option considered was to constantly update the temperature reading in real time. This would be convenient for the user since they would always know the current temperature of the chiller. However, the main purpose is to make sure that the temperature is correct at the beginning of the test. Therefore, having it constantly running is not necessary. Instead, a snapshot method was chosen because it provides all the information the user could need and can get real-time readings as needed. The only fear with this method is that an old reading would be taken as the current temperature and the

test would be started in the wrong conditions. This was fixed by adding the time of the snapshot which updates when the temperature updates.

3.2.2 Interlock System

The purpose of the interlock is to protect the module and testing environment in case of unforeseen events. A software and a hardware interlock is monitoring these tests. The software interlock is constantly fed environmental parameters, such as module temperature, environmental temperature, and humidity, from inside the test jig. It is also fed data from the hardware interlock such as the operating current and voltage. It then displays this data to a web-based interface called Graphana.

The hardware interlock serves as the hard stop to the tests. If the conditions become too poor to continue it will stop the tests by cutting off the power supply to save the module. Meanwhile, if the software monitoring system notices that these parameters approach concerning values, it will email the user and take precautionary methods to change the conditions while keeping the test going. It can take a variety of actions to try and save the test such as ramping down the high voltage, cutting off low voltage, or lowering the chiller temperature. The hardware interlock is only triggered if all else fails.



Figure 12: Interlock Diagram [6]

There is also a watchdog program, which checks that the interlock system is active. It will notify the user if the interlock ceases to work. The watchdog program is necessary for the run of the actual tests.

The purpose of the GUI in this relation is to ensure that all programs are opened in the correct order. If the ordering is not respected then the system of checks does not exist and nothing protects the modules. The GUI is a good tool for this because it can easily forbid certain actions before another is taken. Following Figure 12, the GUI forces the user first

to run the interlock, then watchdog, and only after that can the tests be run. This assures the user that the failure contingencies are correctly set. It also asks the user to fill in fields such as an email to notify in case of issues and a module name.

It is important to tell the user when they are going out of order. The clearest way to communicate this is by having a popup appear on the screen. Simply forbidding an action could confuse the user. The popups appear on top of the main window and block several of the inputs. This way the user is forced to acknowledge the mistake before proceeding. These popups are implemented at every step of the procedure to make sure the user is informed about their mistakes.

3.2.3 Electric Quality Control(QC) Test

The selection of the tests is the most complex part of the GUI because of the variety of options. All possible current tests are displayed in Figure 13, not only is this a lot for a user to remember, but certain tests can be run in multiple ways.

| Scan Option | | | | | | | |
|-------------|-----------------------------|----------------------|--------------|--------------------------|----------------------------|---------------------------|--|
| Module N | ame: | | | | | | |
| | Adc Calibration | Analo | g_readback | SLDO | D 🗌 | IV | |
| mqt | - : Ip-mode | Vcal C | alibration | Inject | tion Capacitance | Over Votlage | |
| | Undershunt | Data 1 | fransmission | Long | Term Stability | | |
| | Digital Scan | Digital Scan M1 | | Analog Scan | Tune Global Threshold 2000 | Tune Pixel Threshold 2000 | |
| yarr: 🗆 | Retune Global Threshhold 15 | 00 Threshold Scan Hi | ۹ 🗆 | Threshold Scan HD | Total Scan | Noise Scan | |
| | Disc Bump Scan | Merged Disc Bum | p Scan 🗌 | Threshold Retune Zero Bi | as Threshold Zero Bias | Source Scan | |
| FullQC Fu | IIQC_noIV ED MHT | TUN PFA p | On 🗌 Verb | oose 🗌 🗆 FEs 🛛 💌 | noAnaED gyc(asn:) | tag: | |
| | Eauo | and Start | | | Hala | | |

Figure 13: GUI for Test Selection

As always, an ASN is required to know which test corresponds to which modules. Undemeath there is the option to select ModuleQCTools(mqt). These are used to perform tests on the modules. Some of the most important ones include the IV test which measures the leakage current through the bulk of the silicon sensors and the long-term stability test which sees if the sensors degrade under long exposures to high voltages. The mqt label can also be changed to analyze the previous results of the tests instead of performing one. Then, yarr scans configure the readout that is obtained from performing the tests.

The last line is special inputs that act differently from the rest. For example, running FullQC runs all of mqt and yarr, running minimal health test(MHT), tuning (TUN), and pixel failure analysis(PFA) is equivalent to all yarr scans.

The electrical tests have several options that perform the same actions or should not be run together. Here, the GUI enforces the hierarchy between them. Only a few inputs are always available. They usually do not affect tests, such as displaying the full outputs or placing a tag on the run. Running analyze, instead of mqt, trumps all other options. Since it only shows previous analysis results, a test would never run at the same time. If analysis options are selected, no other inputs will be run.

Next in line are the last line options, mentioned before, which run multiple options at once. FullQC runs every mqt and yarr scan, so any input there will be disregarded. Same

with MHT, PFA, and TUN but only with yarr.

Because there are many abbreviations, technical terms, and special relationships, the "help" button explains what every option does and how different selections interact with one another. Also, since avoiding errors is the main functionality of the GUI, the user will be prompted to ensure that the hardware interlock is correctly activated. This is a final security check since this is not activated by software. Once that has been confirmed the user can start the test.

Due to the large amount of inputs, the main challenge of this section of the GUI was displaying everything clearly and concisely. The original design (Figure 14) for this window was much different from the one in Figure 13.

The first noticeable difference is the mqt and yarr scans. They were originally textboxes where the user could input whatever tests they wanted. However, this was scraped since it didn't make the test procedure any easier. The user would still be required to write their inputs correctly and know all of the names. Instead, the final design uses check-boxes because it clearly shows the user every option and doesn't require them to remember over 30 of them.

| Scan Option | | | | | | |
|---------------------------------------|--|--|--|--|--|--|
| ASN: | | | | | | |
| ModuleQTools (mqt): | | | | | | |
| yarr: | | | | | | |
| ED MHT TUN PFA FullQC Display Outputs | | | | | | |
| Save and Start Help | | | | | | |

Figure 14: First GUI Design for Test Selection

The last line of checkboxes was also greatly extended. New functionalities were either added as the GUI was being developed or niche pre-exisiting one asked to implemented.

4 Conclusion

The pixel assembly process is still in its early stages. As a result, one of the main goals is to create efficient and effective systems for full production. The current processes are always evolving to better handle modules as new issues are discovered. This is especially true of later stages, such as electric QC, that may not have gotten many working modules yet.

Upgrading to the ITk requires processing plenty of modules. The systems must not only be able to handle them with relative speed but must also take care to find any flaws present before they are put in the detector. From inspecting bare modules for defects to testing new recovery methods to building GUI which makes testing more efficient, my work this summer helped refine the systems currently in place to do just that.

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